Serial No. 10/705,707
Docket : MIO 0100 VA/40509.274

Amendments to the Claims:

This listing of claims will replace all prior versions, and lists, of claims in the application:

1. (Currently amended) A method of forming a memory cell comprising:
   forming a continuous strip of active area on a base substrate;
   forming a trench in said base substrate generally parallel to said strip of active area;
   lining said trench with a first spacer, wherein said first spacer is formed by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide;
   depositing a conductive bit line over said base substrate at least within said trench;
   etching said conductive bit line back below an uppermost surface of said base substrate such that an uppermost surface of said conductive bit line is recessed within said base substrate at least a first distance sufficiently deep to substantially avoid gate induced drain leakage effects;
   forming an insulating capping layer within said trench over said conductive bit line.

2. (Currently Amended) A method of making a memory cell comprising:
   providing a base substrate having an uppermost surface;
   forming a strip of active area on said uppermost surface of said base substrate;
   etching a trench in said base substrate generally along side and adjacent to said strip of active area;
   lining at least a portion of the walls of said trench with a spacer;
   depositing a conductive bit line over said substrate at least within said trench;
   etching said conductive bit line back below an uppermost surface of said base substrate;
   forming a cap within said trench over said conductive bit line, wherein said cap comprises a layer of nitride and a layer of insulating material over said nitride

layer;

forming a transistor, including a first source/drain region and a second source/drain region, in said active area;

coupling a word line to said transistor defining a transistor gate;

coupling a bit line strap between said conductive bit line and said active area at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said transistor.

3. (Original) The method of making a memory cell according to claim 2, further comprising coupling said bit line strap to said first source/drain region through said side wall of said trench.

4. (Currently Amended) A method of making a memory cell comprising:

providing a base substrate having an a first base layer and a second base layer;

forming a strip of active area on said first base layer of said base substrate;

etching a trench in said base substrate generally along side and adjacent to said strip of active area;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back below an uppermost surface of said base substrate such that an uppermost surface of said conductive bit line is recessed at least to an uppermost surface of said second base layer of said base substrate;

forming a cap within said trench over said conductive bit line;

forming a transistor, including a first source/drain region and a second source/drain region, in said active area;

coupling a word line to said transistor defining a transistor gate;

coupling a bit line strap between said conductive bit line and said active area at least

about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said transistor.

5. (Original) The method of making a memory cell according to claim 4, wherein said conductive bit line is recessed below said uppermost surface of said second base layer.

6. (Original) The method of making a memory cell according to claim 4, wherein said first base layer is doped with a first type impurity and said second base layer comprises a buried layer doped with a second type impurity.

7. (Original) The method of making a memory cell according to claim 4, wherein said first base layer comprises a P-type semiconductor material and said second base layer comprises an N+ buried layer.

8. (Original) The method of making a memory cell according to claim 4, wherein said first base layer comprises a semiconductor layer and said second base layer comprises an insulator layer.

9. (Original) The method of making a memory cell according to claim 4, further comprising coupling said bit line strap to said first source/drain region through said side wall of said trench.

10. (Original) A method of making a memory cell comprising:

providing a base substrate having an a first base layer of semiconductor material formed over a second base layer of an insulating material;

forming a strip of active area on said first base layer of said base substrate;

etching a trench in said base substrate generally along side and adjacent to said strip of active area;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back below an uppermost surface of said base substrate such that an uppermost surface of said conductive bit line is recessed below an uppermost surface of said second base layer of said base substrate;

forming a cap within said trench over said conductive bit line;

forming a transistor formed in said active area;

coupling a word line to said transistor defining a transistor gate;

coupling a bit line strap between said conductive bit line and said active area at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said transistor.

11. (Cancelled)

12. (Currently amended) ~~The method of making a memory cell according to claim 11,~~ A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a first type well within said base substrate;

forming a transistor in said first type well comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back below said uppermost surface of said base substrate, wherein said bit line is recessed below said uppermost surface of said base

substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

13. (Currently amended) The method of making a memory cell according to claim ~~11~~12, wherein said trench is etched to a depth greater than twice a minimum realizable feature size.

14. (Currently amended) The method of making a memory cell according to claim ~~11~~12, wherein said spacer is formed by:

thermally growing a first layer of oxide;

depositing a second layer of oxide over said first layer of oxide; and

depositing a nitride layer over said second layer of oxide.

15. (Currently amended) The method of making a memory cell according to claim ~~11~~12, wherein said spacer is formed so as to have a thickness of approximately one fourth the minimum realizable feature size.

16. (Currently amended) The method of making a memory cell according to claim ~~11~~12, wherein said cap layer is formed by:

forming a capping layer of nitride over said conductive bit line; and

forming a capping insulating material of HDP over said nitride.

17. (Currently amended) The method of making a memory cell according to claim ~~11~~12, further

comprising coupling said bit line strap to said first source/drain region through a side wall of said trench.

18. (Cancelled)

19. (Currently amended) ~~The method of making a memory cell according to claim 18,~~ A method of making a memory cell comprising:

providing a base substrate having an a first base layer of semiconductor material and a second base layer of semiconductor material;

forming a transistor on said base substrate comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate passing generally adjacent to said transistor;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that an uppermost surface of said conductive bit line is recessed at least to an uppermost surface of said second base layer of said base substrate, wherein said bit line is recessed below said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

20. (Currently amended) The method of making a memory cell according to claim ~~18~~19, wherein

said trench is etched to a depth greater than twice a minimum realizable feature size.

21. (Currently amended) The method of making a memory cell according to claim ~~18~~19, wherein said spacer is formed by:

thermally growing a first layer of oxide;

depositing a second layer of oxide over said first layer of oxide; and

forming a nitride layer over said second layer of oxide.

22. (Currently amended) The method of making a memory cell according to claim ~~18~~19, wherein said spacer is formed so as to have a thickness of approximately one fourth the minimum realizable feature size.

23. (Currently amended) The method of making a memory cell according to claim ~~18~~19, wherein said cap layer is formed by:

forming a capping layer of nitride over said conductive bit line; and

forming a capping insulating material of HDP over said nitride.

24. (Currently amended) The method of making a memory cell according to claim ~~18~~19, further comprising coupling said bit line strap to said first source/drain region through a side wall of said trench.

25. (Cancelled)

26. (Currently amended) ~~The method of making a memory cell according to claim 25,~~ A method of making a memory cell comprising:

providing a base substrate having an a first base layer of semiconductor material over a second base layer of insulating material;

forming a transistor on said base substrate comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate passing generally adjacent to said transistor;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that an uppermost surface of said conductive bit line is recessed below an uppermost surface of said second base layer of said base substrate, wherein said bit line is recessed below said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

27. (Currently amended) The method of making a memory cell according to claim ~~25~~26, wherein said trench is etched to a depth greater than twice a minimum realizable feature size.

28. (Currently amended) The method of making a memory cell according to claim ~~25~~26, wherein said cap layer is formed by:

forming a capping layer of nitride over said conductive bit line; and

forming a capping insulating material of HDP over said nitride.

29. (Currently amended) The method of making a memory cell according to claim ~~25~~26, further comprising coupling said bit line strap to said first source/drain region through a side wall of said

trench.

30. (Currently amended) A method of making a memory cell comprising:

forming a base substrate having an uppermost surface;

forming a p-type well within said base substrate;

forming a transistor in said p-type well comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate, wherein said bit line is recessed below said uppermost surface of said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

31. (Currently amended) A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a first type well within said base substrate;

forming a transistor in said first type well comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate, wherein said bit line is recessed below said uppermost surface of said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

implanting a first type doping in said first type well at least about a portion of said well adjacent said portion of said trench containing said conductive bit line, said first type doping of the same type as said first type well and in a concentration sufficiently high to prevent inversion;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

32. (Original) The method of making a memory cell according to claim 31, further comprising coupling said bit line strap to said first source/drain region through said side wall of said trench.

33. (Currently amended) A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a P-type well within said base substrate;

forming an N-type active area within said P-type well

etching a trench in said base substrate passing generally adjacent to said N-type active

area;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate, wherein said bit line is recessed below said uppermost surface of said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming an insulating cap within said trench over said conductive bit line; and

coupling a bit line strap between said conductive bit line to said N-type active area about said uppermost surface of said substrate and through said side wall of said trench.

34. (Currently amended) A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a strip of active area on said uppermost surface of said base substrate;

etching a trench in said base substrate generally along side and adjacent to said strip of active area;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that an uppermost surface of said conductive bit line is recessed below an uppermost surface of said base substrate;

forming a cap within said trench over said conductive bit line, wherein said cap comprises a layer of nitride and a layer of insulating material over said nitride layer;

forming a transistor in said active area;

coupling a word line to said transistor defining a transistor gate;

coupling a bit line strap between said conductive bit line and said active area at least

about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said transistor.

35. (Original) A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a strip of active area on said uppermost surface of said base substrate;

forming a transistor in said active area comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate generally along side and adjacent to said strip of active area;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that an uppermost surface of said conductive bit line is recessed within said substrate at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

36. (Currently amended) A method of making a memory cell comprising:

providing a base substrate having an uppermost surface;

forming a strip of active area on said uppermost surface of said base substrate;

forming a transistor in said active area comprising a channel separated between a first

source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate generally parallel to and along side said strip of active area;

forming a spacer within said trench lining at least a portion of the walls of lining at least a portion of the walls of said trench with a spacer, wherein said spacer is formed by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide;

depositing a conductive bit line over said base substrate at least within said trench;

etching said conductive bit line back below said uppermost surface of said base substrate a distance arranged to substantially eliminate a gate induced drain leakage of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.

37. (Currently amended) A method of making a memory cell pair comprising:

providing a base substrate having an a first base layer and a second base layer;

forming a strip of active area on said first base layer of said base substrate;

forming a pair of transistors in said strip of active area, each of said transistors sharing a common first source/drain region, a channel separated between said common first source/drain region and a second source/drain region;

coupling a word line to said channel of each one of said pair of transistors;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said second base layer, wherein said bit line is recessed below said uppermost surface of said base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of said transistor;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said common first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a pair of capacitors over said base substrate; and

electrically coupling each of said pair of capacitors to an associated one of said second source/drain regions.

38. (Original) A method of making a memory cell pair comprising:

providing a base substrate having an a first base layer of semiconductor material formed over a second base layer of an insulating material;

forming a strip of active area on said first base layer of said base substrate;

forming a pair of transistors in said strip of active area, each of said transistors sharing a common first source/drain region, a channel separated between said common first source/drain region and a second source/drain region;

coupling a word line to said channel of each one of said pair of transistors;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that an uppermost surface of said conductive bit line is recessed below an uppermost surface of said second base layer of said

base substrate;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said common first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a pair of capacitors over said base substrate; and

electrically coupling each of said pair of capacitors to an associated one of said second source/drain regions.

39. (Currently amended) A method of making a memory array comprising:

providing a base substrate having an uppermost surface;

forming a strip of active area on said base substrate;

forming a plurality of pairs of transistors in said strip of active area, each of said pairs of transistors sharing a common first source/drain region and further comprising a channel separated between said common first source/drain region; and a second source/drain region;

coupling a word line to said channel of each transistor defining a transistor gate;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate;

forming a cap within said trench over said conductive bit line, wherein said cap comprises a layer of nitride and a layer of insulating material over said nitride layer;

forming a plurality of bit line contact straps, each bit line contact strap coupled between said conductive bit line and an associated one of said common first source/drain

regions of said transistor at least about said uppermost surface of said substrate;

forming a plurality of capacitors over said substrate;

coupling each capacitor to an associated one of said second source/drain regions.

40. (Currently amended) A method of making a memory cell array comprising:

providing a base substrate having an uppermost surface;

forming a first strip of active area doped to define at least a first source/drain region, a first channel, a second source/drain region, a second channel, a third source/drain region, a third channel, a fourth source/drain region, a fourth channel, a fifth source/drain region, a fifth channel and a sixth source/drain region;

etching a first trench in said base substrate generally adjacent to said first strip of active area;

lining at least a portion of the walls of said first trench with a spacer, wherein said spacer is formed by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate;

forming a capping layer within said trench over said bit line;

coupling a first word line to said first channel such that a first transistor is defined by said first source/drain region, said first channel and said second source/drain region;

forming a first capacitor over said base substrate;

coupling said first capacitor to said first source/drain region;

coupling a second word line to said second channel such that a second transistor is defined by said second source/drain region, said second channel and said third source/drain region;

forming a second capacitor over said base substrate;

coupling said second capacitor to said third source/drain region;

coupling a first conductive layer to said third channel;

coupling said first conductive layer to a first reference voltage;

coupling a third word line to said fourth channel such that a third transistor is defined by said fourth source/drain region, said fourth channel and said fifth source/drain region;

forming a third capacitor over said base substrate;

coupling said third capacitor to said fourth source/drain region;

coupling a fourth word line to said fifth channel such that a fourth transistor is defined by said fifth source/drain region, said fifth channel and said sixth source/drain region;

forming a fourth capacitor over said base substrate;

coupling said fourth capacitor to said sixth source/drain region;

coupling a first bit line contact strap between said bit line and said second source/drain region at least about said uppermost surface of said substrate; and

coupling a second bit line contact strap between said bit line and said fifth source/drain region at least about said uppermost surface of said substrate.

41. (Original) The method of making a memory cell according to claim 40, wherein said first reference voltage comprises ground potential.

42. (Currently amended) A method of making a computer system comprising:

providing a processor;

providing at least one storage device communicably coupled to said processor;

providing at least one input/output device communicably coupled to said processor

providing a memory device communicably coupled to said processor, said memory device having at least one memory cell formed by:

providing a base substrate having an uppermost surface;

forming a strip of active area on said base substrate;

forming a transistor in said strip of active area comprising a channel separated between a first source/drain region and a second source/drain region;

coupling a word line to said channel of said transistor defining a transistor gate;

etching a trench in said base substrate;

lining at least a portion of the walls of said trench with a spacer, wherein said spacer is formed by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide;

depositing a conductive bit line over said substrate at least within said trench;

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate;

forming a cap within said trench over said conductive bit line;

coupling a bit line strap between said conductive bit line and said first source/drain region of said transistor at least about said uppermost surface of said substrate;

forming a capacitor over said substrate; and

electrically coupling said capacitor to said second source/drain region.